SUDHANSHU GUPTA (HE/HIM)

Silicon Performance Architect, Meta Reality Labs
1180 Discovery Way ⋄ Sunnyvale, CA 94089

sudhanshu96@meta.com sudhanshu-gupta-in sacusa

OVERVIEW

I am a systems researcher specializing in computer architecture and low-level software design, interested in the co-design of hardware and software aimed at improving the performance and efficiency of processors.

EDUCATION

University of Rochester, NY, USA August 2019 - August 2025
Ph.D., Computer Science GPA: 3.75/4.00
Dissertation: Managing Data Movement Bottlenecks in Accelerator-Rich Systems
Advisor: Prof. Sandhya Dwarkadas

University of Rochester, NY, USA August 2019 - May 2021
M.S., Computer Science GPA: 3.82/4.00

NIIT University, RJ, India July 2015 - July 2019
B.Tech., Computer Science and Engineering CGPA: 8.87/10.00

EXPERIENCE

Meta Platforms August 2025 - Present
Silicon Performance Architect, Meta Reality Labs *Sunnyvale, CA, USA*

- Building the next generation of XR devices with the SoC Creations Team at Meta Reality Labs.

University of Rochester August 2019 - August 2025
Graduate Research Assistant, advised by Prof. Sandhya Dwarkadas *Rochester, NY, USA*

- Investigated data movement issues in current and future processors, focusing on:
  1. Accelerator scheduling to reduce off-chip data movement and provide quality-of-service.
  2. Interconnect and memory controller design for PIM-enabled processors.
  3. Characterizing the impact of emerging heterogeneous memory on accelerator performance.

AMD Research May 2022 - December 2022
Intern/Co-op, Core and SoC Architecture Team *Austin, TX, USA*

- Contributed to the interconnect/memory controller interface for future architectures.
- Explored memory controller scheduling for PIM-enabled architectures.

Indian Institute of Technology, Delhi January 2019 - July 2019
Research Intern, supervised by Prof. Smruti Ranjan Sarangi *New Delhi, DL, India*

- Designed a benchmark suite sporting state-of-the-art CNN-based autonomous driving applications.
- Extended *Tejas* simulator to characterize compute and memory deficiencies in modern out-of-order CPUs, demonstrating CPUs outperforming GPUs in multi-application scenarios.

Indian Institute of Technology, Kanpur May 2018 - July 2018
Research Intern (SURGE), supervised by Prof. Biswabandan Panda *Kanpur, UP, India*

- Studied memory subsystem optimizations for machine learning applications running on CPUs.
- Characterized the memory performance of emerging machine learning applications using *ChampSim* simulator, demonstrating the inefficacy of state-of-the-art cache prefetchers.

PUBLICATIONS

1. **S. Gupta** and S. Dwarkadas, "Improving the Performance of Out-of-Core LLM Inference Using Heterogeneous Host Memory," *2025 IEEE International Symposium on Workload Characterization (IISWC)*, Irvine, CA, USA, 2025, *to appear*.
2. **S. Gupta**, N. Madan, S. Puthoor, N. Jayasena and S. Dwarkadas, "Concurrent PIM and Load/Store Servicing in PIM-Enabled Memory," *2025 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Ghent, Belgium, 2025, pp. 320-334, doi: 10.1109/ISPASS64960.2025.00037.
3. **S. Gupta** and S. Dwarkadas, "RELIEF: Relieving Memory Pressure In SoCs Via Data Movement-Aware Accelerator Scheduling," *2024 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, Edinburgh, United Kingdom, 2024, pp. 1063-1079, doi: 10.1109/HPCA57654.2024.00084.
4. D. Moolchandani, **S. Gupta**, A. Kumar and S. R. Sarangi, "Performance Prediction for Multi-Application Concurrency on GPUs," *2020 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Boston, MA, USA, 2020, pp. 306-315, doi: 10.1109/ISPASS48437.2020.00050.

TECHNICAL SKILLS

- **Computer languages:** C, C++, CUDA, Python, Java, Bash, OpenMP, MPI, Verilog
- **Architectural simulators:** gem5, gem5-SALAM, gem5-Aladdin, GPGPU-Sim, ChampSim, Tejas
- **Tools:** Intel Pin, Perf, Git, Valgrind, GDB, Nvidia NSight

PROFESSIONAL SERVICE

- Facilitated **ISCA 2024 Program Committee** meetings.
- **Artifact Evaluation Committee:** ISCA 2024, ISCA 2023

TEACHING EXPERIENCE

University of Rochester Rochester, NY, USA

- Teaching Assistant for CSC 252: Computer Organization (Spring 2020, Fall 2020, Spring 2021)

NIIT University Neemrana, RJ, India

- Teaching Assistant for CS 382: Programming Tools (Fall 2018)

Indian Institute of Technology, Kanpur Kanpur, UP, India

- Teaching Assistant Computer Architecture Summer School 2018 (Summer 2018)

COMMUNITY

University of Rochester Rochester, NY, USA

- Serving in the Graduate Labor Union Organizing Committee.
- Computer Science Events Committee co-chair.

NIIT University Neemrana, RJ, India

- Technical Lead at FOSS Society, an umbrella society housing the Firefox Community and Linux Users Group.
- Founder and Club Lead at Linux Users Group, a group of enthusiastic users and learners of Linux.
- Member of President's Student Advisory Board, advising the president on student affairs.